**Project 5 Evaluation**

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| Name: | | Total: | |
| Checklist | Weight | Earned | Notes |
| 1. Description of QRD design architecture | 10 |  |  |
| 1. Model Composer model using the Vitis HLS block and testing results. | 30 |  |  |
| 1. Generate IP block from Model Composer and integrate with ARM processor using Vivado. Generate hardware and XSA for Vitis | 20 |  |  |
| 1. Vitis C++ control of QRD Model Composer accelerator with testing results of at least 2 test matrices | 20 |  |  |
| 1. Synthesis and place and route implementation report from Vivado. | 10 |  |  |
| 1. Turning in files including Model Composer file, screen capture of Vivado block diagram, Vitis C++ file, and screen capture of Vitis terminal results | 10 |  |  |